

Minutes of TMAG Test Economics Committee
12 February 2010
Minutes by Scott Davidson

Attendees:

Tony Ambler
Scott Davidson
Jack George
Tom Maiello
Russell Shannon
Louis Ungar

Tom, the special guest for this meeting, is Test Program Set Chief at Picatinny.

Tom said each LRU has some level of built-in test. It will be a requirement for each component, but the quality varies depending on the supplier. Each vendor will say they will meet the requirements, but how well they meet requirements of detecting all detectable faults varies.

How to do system test is another problem. BIT doesn't isolate, which is tough. BIT runs inside a system, and does not have to be run standalone. Maintenance requirements are to box level.

How to measure quality? False alarm rate in the field? Sampling of small set of faults during demonstrations. There might not be enough time to test for all "relevant" faults – could be a thousand, but the Navy only can do 10 or 20, and sometimes not even that. In addition, the vendor selects the subset of faults to be inserted.

Fault lists come from the vendor, or perhaps from the government. The faults of interest are basically defined by the contract.

We discussed the problem of fault models and simulation, and the problem of not enough samples. Many of the failures they see in the field are things not anticipated, like wire chafing in helicopters.

FMICAs are good, but there are many gaps in them. According to Tom, FMICAs are useful, but even when a fault is considered they cannot always prove it will be detected. In one example, a FMICA was done but no one knew the impact of the fault. He would like a demonstration that all the faults are caught. The 20 faults considered during a demonstration are not enough for this.

Scott suggested that simulation might be used to test for detection of a larger number of faults than can be done during a demonstration. Russell and Tom said that they would still want to see detection in the hardware. It appears that the biggest problems found are in the interfaces and in parts from different vendors not interoperating well.

Some faults, such as shorts and opens, would be relatively easy to simulate and insert. It is not known how a certain coverage on this set of faults maps into coverage of actual faults.

Tony asked if we could formally verify the interfaces between the boxes. Given that this is the biggest issue, we'd only have to consider the source interface logic, cable, and destination interface logic. It is not

clear that anyone has done verification taking these analog issues into account.

Russell requested a short primer – 5 slides or so - to discuss testability. He will send what his managers need to see, and we will create some slides to put on the website which we hope will meet this need.

Ais:

Scott: Put Tom on the mailing list. Done

Russell: Send a description of what is needed for a testability talk

Scott/Tony: Find some references about formal verification of interfaces. Scott has found one possibility.